**CSE 458 Lab Final**

**Full Marks: 40 Time: 1 Hour**

1. **Crux** = (Your registration number) **MOD** (7)

Write a Verilog code such that it has **3 inputs** and **1 output**. The three inputs represent a decimal value (from 0 to 7) and output is 1 if the value is greater than **Crux** else it is 0.

Test all 8 possibility in your testbench.

(check example at the bottom if you are confused).

**Upload the following to classroom**

* 1. Verilog code in .v format 10
  2. Testbench code in .v format 5
  3. Screenshot of the output in .png format 5

1. Draw the schematic diagram of the following function in DSCH.

F = ( A B + C ) D

Now, produce the function’s layout in microwind using Verilog code that you obtain from DSCH.

**Upload the following to classroom**

* 1. DSCH file in .sch format 10
  2. Microwind file in .msk format 5
  3. Screenshot of the simulation in .png format 5

Example of 1.

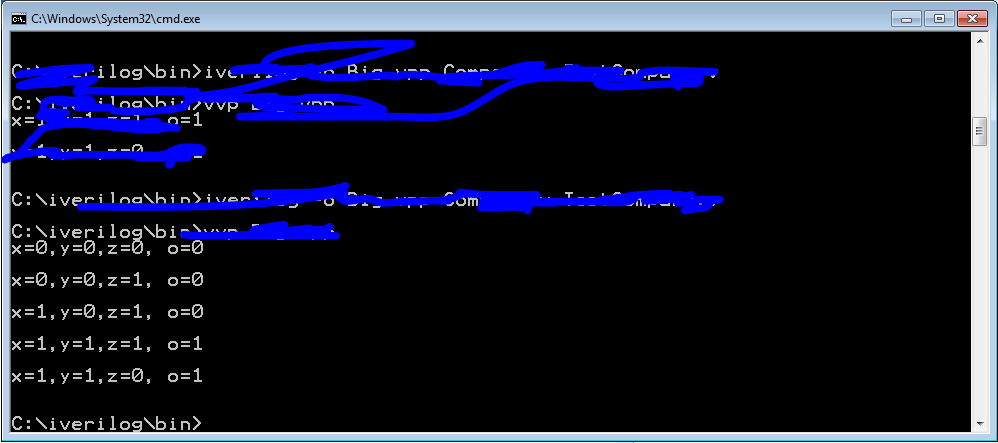
My registration number is 0000005

So, Crux = 5

So, it will produce the following table:

|  |  |  |  |
| --- | --- | --- | --- |
| X | Y | Z | OUTPUT |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 |

And so on …..



**You should test all 8 cases.**